What is claimed is:

1. A semiconductor memory device having semiconductor memory chips, each semiconductor memory chip comprising:

a plurality of memory banks capable of independently to be accessed, each memory bank having a plurality of memory blocks, wherein at least two memory blocks, which are adjacent each other in the same memory bank, have the different number of unit memory blocks, so that each bank has a non-rectangular shape.

2. The semiconductor memory device as recited in claim 1, further comprising a plurality of pads and control blocks arranged in a vacant space between neighboring memory banks.

3. The semiconductor memory device as recited in claim 1, wherein each of memory blocks includes a pair of X-decoder and Y-decoder.

4. The semiconductor memory device as recited in claim 1, wherein each memory bank includes odd numbers of memory blocks.

5. The semiconductor memory device as recited in claim 1, wherein a total memory region of the semiconductor memory chip is divided into four memory banks, wherein four memory banks are arranged to the first, second, third and fourth quadrants of the semiconductor memory chip, respectively.

6. The semiconductor memory device as recited in claim 5, wherein each memory bank includes:

a first memory block having first numbers of unit memory blocks;

a second memory block having second numbers of unit

memory blocks, which is smaller than that of the first memory blocks; and

a third memory block having the second numbers of unit memory blocks.

7. The semiconductor memory device as recited in claim 6, wherein the first memory blocks of memory banks arranged in the second and third quadrants are arranged at a left-most region of the semiconductor memory chip and the first memory block of banks arranged in the first and fourth quadrants is arranged at a right-most region of the semiconductor memory chip.

8. The semiconductor memory device as recited in claim 7, further comprising a plurality of pads and control blocks arranged between the neighboring second memory blocks, which belong to different memory banks, wherein the pads are arranged between the neighboring first memory blocks.

9. The semiconductor memory device as recited in claim 6, wherein each first memory block of each memory bank is arranged by being neighbored in a central region of the semiconductor memory chip.

10. The semiconductor memory device as recited in claim 9, further comprising a plurality of pads and control blocks arranged between the neighboring second memory blocks, which belong to different memory banks, wherein the pads are arranged between the neighboring first memory blocks.

11. The semiconductor memory device as recited in claim 6, wherein each first memory block of each memory bank is arranged in a central region of each bank, respectively.

12. The semiconductor memory device as recited in claim 11, further comprising a plurality of pads and control blocks arranged between the neighboring second memory blocks, which belong to different memory banks, wherein the pads are arranged between the neighboring first memory blocks.

13. The semiconductor memory device as recited in claim 6, wherein each of the first, second and third memory blocks has a pair of X-decoder and Y-decoder, respectively, and a final driving terminal of the X-decoder in the first memory blocks is separated into two driving terminals.

14. The semiconductor memory device as recited in claim 6, wherein the first memory block includes six 8-Mbit unit memory blocks and the second and the third memory blocks includes five 8-Mbit unit memory blocks.

15. The semiconductor memory device as recited in claim 5, wherein each memory bank includes:

a first memory block having a first numbers of unit memory blocks;

a second memory block having a second numbers of unit memory blocks, which is smaller than that of the first memory block; and

a third memory block having the first numbers of unit memory blocks.

16. The semiconductor memory device as recited in claim 15, wherein the second memory blocks of memory banks arranged in the second and third quadrants are arranged at a left-most region of the semiconductor memory chip and the second memory blocks of banks arranged in the first and fourth quadrants are arranged at a right-most region of the semiconductor memory chip.

17. The semiconductor memory device as recited in claim 16, further comprising a plurality of pads and control blocks arranged between the neighboring second memory blocks, which belong to different memory banks, wherein the pads are further arranged between the neighboring first memory blocks.

18. The semiconductor memory device as recited in claim 15, wherein each second memory block of each memory bank is arranged by being neighbored in a central region of the semiconductor memory chip.

19. The semiconductor memory device as recited in claim 18, further comprising a plurality of pads and control blocks arranged between the neighboring second memory blocks, which belong to different memory banks, wherein the pads are further arranged between the neighboring first memory blocks.

20. The semiconductor memory device as recited in claim 15, wherein each second memory block of each memory bank is arranged in a central region of each bank, respectively.

21. The semiconductor memory device as recited in claim 20, further comprising a plurality of pads and control blocks arranged between the neighboring second memory blocks, which belong to different memory banks, wherein the pads are further arranged between the neighboring first memory blocks.

22. The semiconductor memory device as recited in claim 15, wherein each of the first, second and third memory blocks has a pair of X-decoder and Y-decoder, respectively, and a final driving terminal of the X-decoder in the first and the third memory blocks is separated into

two driving terminals.

23. The semiconductor memory device as recited in claim 15, wherein each of the first and the third memory blocks includes six 8-Mbit unit memory blocks and the second memory blocks includes five 8-Mbit unit memory blocks.

24. A semiconductor memory device having a semiconductor memory chip divided into 18 regions having an equal area in a 3 rows X 6 columns array, the semiconductor memory chip comprising:

a first memory bank including memory blocks arranged at one region selected from a 2^{nd} row X 1^{st} column region, a 2^{nd} row X 2^{nd} column region and a 2^{nd} row X 3^{rd} column region and at a 1^{st} row X 1^{st} column region, a 1^{st} row X 2^{nd} column region and a 1^{st} X 3^{rd} column region;

a second memory bank including memory blocks arranged at one region selected from a 2^{nd} row X 1^{st} column region, a 2^{nd} row X 2^{nd} column region and a 2^{nd} row X 3^{rd} column region and at a 3^{rd} row X 1^{st} column region, a 3^{rd} row X 2^{nd} column region and a 3^{rd} X 3^{rd} column region;

a third memory bank including memory blocks arranged at one region selected from a 2^{nd} row X 4^{th} column region, a 2^{nd} row X 5^{th} column region and a 2^{nd} row X 6^{th} column region and at a 1^{st} row X 4^{th} column region, a 1^{st} row X 5^{th} column region and a 1^{st} X 6^{th} column region;

a fourth memory bank including memory blocks arranged at one region selected from a 2^{nd} row X 4^{th} column region, a 2^{nd} row X 5^{th} column region and a 2^{nd} row X 6^{th} column region and at a 3^{rd} row X 4^{th} column region, a 3^{rd} row X 5^{th} column region and a 3^{rd} X 6^{th} column region; and

pads and control blocks arranged at one region selected from the 2^{nd} row X 1^{st} column region, the 2^{nd} row X 2^{nd} column region, the 2^{nd} row X 3^{rd} column region, the 2^{nd} row X 4^{th} column region, the 2^{nd} row X 5^{th} column region and

the 2nd row X 6th column region.

25. The semiconductor device as recited in claim 24, wherein a X-decoder between the neighboring memory blocks in the same memory bank is shared each other.

26. The semiconductor device as recited in claim 24, wherein the pads are arranged between the first and second banks and the third and fourth banks.

27. A method for arranging memory blocks to a semiconductor memory chip in a semiconductor device, comprising of:

configuring a plurality of memory blocks with a plurality of neighboring unit memory blocks; and

configuring a plurality of memory banks with the neighboring memory blocks, wherein at least two memory blocks have different numbers of unit memory blocks each other in the same bank so that each memory bank has a non-rectangular shape.

28. The method as recited in claim 27, wherein pads and control blocks are arranged between the memory blocks relatively having smaller number of unit memory blocks.